CLAIMS

1. A method for providing an improved integrated circuit device comprising the steps of:

providing active and passive areas in the substrate,

providing a plurality of slots in the substrate after providing the active and passive areas, oxidizing the plurality of slots; and

providing metal in each of the plurality of slots and,

providing a dielectric coating over the slots and the remaining silicon; and

providing etched contacts in select areas remote from the location of the buried power buss (BPB); and

providing an additional layer of metal that interconnects the contacts and the buried metal in select areas where contacts were opened (power buss), resulting in metal of three levels and

providing triple metal technology with one layer on the top surface consisting of a single layer of metal, one layer that is buried consisting of two layers of metal buried power buss (BPB), and the power buss (PB) that has three layers of metal located where contacts were opened prior to the final metal deposition; all while providing single metal processing and patterning of a single thin metal.

2. The method of claim 1 wherein the triple metal technology providing steps comprising the step of three independent oxide isolated metal layers being of sufficient thickness to carry high current.

3. The method of claim 1 wherein the slots are placed in a manner that minimizes the process steps for manufacture.

4. The method of claim 1 wherein the high temperature and long time process of the junction isolation is eliminated.

5. The method of claim 1 wherein the high temperature and long time process of the sinker is eliminated.

6. The method of claim 1 wherein active and passive areas are provided for bipolar, CMOS, BICMOS, DMOS and BCD technologies with improved properties.

7. The method of claim 1 wherein select slots are opened in the dielectric prior to metal to allow the oxide to be removed from the bottom of slots that are to make ground contact to the substrate and metal contact to the buried layer to replace the sinker.

8. The method of claim 1 wherein oxide isolation is provided versus junction isolation.

9. The method of claim 1 three layers of metal are provided with only one layer of metal requiring masking and pattern etching.

10. The method of claim 1 wherein the design critical dimensions between active and passive areas can be significantly reduced and in many cases can touch, providing a significant reduction in the die size of any of the technologies is provided.

11. The method of claim 1 wherein coupling capacitances are greatly reduced as a result of oxide isolation versus junction isolation.

12. The method of claim 1 whereby the slots are ideally located to provide significant parametric advantages for the various technologies.

13. The method of claim 1 whereby the slots are ideally located to provide significant circuit advantages for the various technologies.

14. The method of claim 1 whereby the slots are ideally located to provide significant system advantages for the various technologies.

15. The method of claim 1 whereby one obtains three layers of thick metal of three different thicknesses, each isolated from one another, while only requiring to etch a single thin layer (the last deposited).

16. The method of claim 1 whereby three layers of isolated metal interconnect are formed while only requiring one layer of dielectric to be deposited and contact etched, versus standard triple metal processes which requires three layers of dielectric to be deposited and contact (or via) etched.

17. The method of claim 1 whereby one obtains two very thick layers of metal in the buried power buss (BPB) and three layers of metal in the power buss (PB) and a single layer of metal on the top surface without metal having to cross over high metal steps (which cause metal to break).

18. The method of claim 1 whereby the high current is carried on the buried power buss (BPB) and power buss (PB) with their thick metals and the third layer is for interconnection of low power circuitry.

19. The method of claim 1 which provides improved parameters for bipolar, CMOS, BICMOS, Shottky diodes and solar cells as listed below:

(a) lower on resistance (RON) for circuits containing:

1. bipolar transistor collectors and emitters
2. CMOS transistor sources and drains
3. lateral PNP collectors and emitters
4. BICMOS which contains bipolar and CMOS transistors and advantages listed for each.
5. DMOS sources and drains (vertical and lateral DMOS)

(b) reduction of capacitance of:

1. collector output capacitance (bipolar)

2. collector to base capacitance of bipolar transistors

3. drain capacitance of CMOS and MOS transistors